VadaTech AMC72X

User's Manual

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vadatech inc

THE POWER OF VISION

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Revision History

Doc Rev	Description of Change	Revision Date
1.0.0	Document Created	3/26/2013
1.2.0	Updated Serial over lan	4/20/2013
1.3.0	Added network device mapping section	5/20/2013
1.4.0	Updated Default Switch Settings	6/14/2013
1.5.0	Updated Network boot (PXE) configuration instructions	6/19/2013
1.6.0	Added instructions for AMI AFU BIOS upgrade	6/26/2013
1.7.0	Updated Linux software section	8/22/2013
1.8.0	Changed SW3-4 default to Off (On-Board Clock)	2/01/2014
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2.0.0	Updated with AMC725 related information	04/30/2014
2.1.0	Added VNC server support	08/09/2014

Table of Contents

1 Overview 7
1.1 Applicable Products 7
1.2 Document References 7
1.3 Acronyms Used in this Document 8
2 Hardware Overview 9
2.1 Block Diagram 9
2.2 Board Layout 10
2.3 Front Panel Layouts 11
2.4 Temperature Sensors 12
3 IPMI Management Interface 13
3.1 IPMI Internal 10/100 Ethernet 14
4 DIP Switch Settings 15
4.1.1 IPMI Related functions 15
4.1.2 Write Protection Switches 15
4.1.3 Board Configuration Switches 15
4.1.4 SRIO Configuration Switches 16
5 Gladden Interface 17
5.1 Serial Console Port 17
5.2 USB Ports 17
5.3 1GbE Ports 18
5.4 XAUI Ports (only applicable to AMC721 and AMC723) 18
5.5 SRIO Ports (only applicable to AMC722) 19
5.6 SD Card Socket 19
5.7 CaveCreek EEPROM 20
5.8 DDR3 SO-DIMMs 20
5.9 Ethernet PHY Addressing 21
6 Software 22
6.1 BIOS 22
6.2 Linux 25
6.3 Graceful Shutdown Support 26
6.3.1 Implementing Graceful Shutdown 27
7 IPMI E-Keying Configuration 28
8 Serial Over Lan (SOL) 29
9 Factory Setup 30
9.1 Initial Factory Setup 30
9.2 Writing the Factory Default SD Card Contents 30
10 AMC725 Specific Changes 32
10.1 Block Diagram 32
10.2 Summary 32
10.3 Switches and Sensors 33

Figures

Figure 1: AMC72X (applicable to X=0, 1, 2, and 3) Block Diagram 9
Figure 2: AMC72X Top Layout (front to the left) (X=0, 1, 2, and 3) 10
Figure 3: AMC72X Bottom Layout (front to the left) (X=0, 1, 2, and 3) 10
Figure 4: AMC720 Front Panel 11
Figure 5: AMC721 Front Panel 11
Figure 6: AMC722 Front Panel 11
Figure 7: AMC723 Front Panel 12
Figure 8: AMC725 Front Panel 12
Figure 9: Temperature Sensor Location (Bottom Side of AMC72X Board) (X=0, 1, 2, and 3) 12
Figure 10: AMC725 Block Diagram 32
Figure 11: AMC725 PCB Top Side 33
Figure 12: AMC725 PCB Bottom Side 34

Tables

Table 1: Acronyms....8
Table 2: AMC72X Switch configurations....11
Table 3: AMC LED Behavior....13
Table 4: IPMI RS232 connector pin-out....14
Table 5: SW2 settings....15
Table 6: Write Protection Switch Settings....15
Table 7: Board Configuration Switch Settings....16
Table 8: SRIO Configuration Switch Settings....16
Table 9: SRIO Base Device ID Control Switch Settings....16
Table 10: SRIO Speed Settings....16
Table 11: CPU RS232 connector pin-out....17
Table 12: USB port pin-out....17
Table 13: ETH0 LEDs....18
Table 14: ETH1 LEDs....18
Table 15: 10GbE LEDs....18
Table 16: SRIO Bridge LEDs....19
Table 17: SD Card LED....19
Table 18: DDR3 SO-DIMM mapping....20
Table 19: Gladden Ethernet PHY Addressing....21
Table 20: AMC720 and AMC722 Network Device Mapping....25
Table 21: AMC721 Network Device Mapping....25
Table 22: AMC723 Network Device Mapping....26
Table 23: Graceful Shutdown IPMI OEM Commands....27
Table 24: AMC720 E-Keying Configuration....28
Table 25: AMC722 E-Keying Configuration....28

1 Overview

The AMC72X are Processor AMC (PrAMC) modules in a single or double-width (based on model), mid or full-height AdvancedMC (AMC) form factor based on the Intel® next generation Core i Processor (Gladden) with Cave Creek PCH

This document describes the VadaTech AMC72X boards and their use as a development platform.

This boards feature:

- Intel Gladden processor options for 1, 2 or 4 cores
- Core speed options ranging from 1 GHz to 2GHz
- Options for 4GB, 8GB, or 16GB of DDR3 ECC memory (dual slot/single controller)
- PCIe, SRIO or XAUI to the backplane fabric 4-7 and 8-11
- Four 1GbE ports
    - Two dedicated as 1000Base-X AMC Port 0 and Port 1
    - Two dedicated as ETH0 and ETH1 front 10/100/1000Base-T ports
- SD card slot on-board for file system storage (USB2244)
- 8MB of boot flash memory standard (AT25DF321A)
- Dual SATA Ports to AMC Port 2 and Port 3
- Dual USB on the front panel
- Real-time Clock with battery backup
- RS-232 serial console on the front panel
- On-board AMC MMC IPMI management controller
- Serial Over LAN (SOL) – Gladden console via the MMC IPMI Ethernet on one of four 1GbE Ports (software configurable from CLI)
- Hardware random number generator for enhanced SOL cryptographic security

1.1 Applicable Products

- VadaTech AMC720
- VadaTech AMC721
- VadaTech AMC722
- VadaTech AMC723
- VadaTech AMC725

1.2 Document References

- PICMG AMC.0 (base) standard

- PICMG AMC.1 (PCIe) standard
- PICMG AMC.2 (Ethernet) standard
- PICMG AMC.4 (SRIO) standard
- VadaTech AMC72X Datasheet

1.3 Acronyms Used in this Document

Acronym	Description
AMC	Advanced Mezzanine Card
ATCA	Advanced Telephony Computing Architecture
BSP	Board Support Package
CPU	Central Processing Unit
DDR	Double Data Rate
DIP	Dual In-line Package
ECC	Error Correction Coding
GB	Gigabyte
GbE	Gigabit Ethernet
GHz	Gigahertz
GND	Ground
IPMI	Intelligent Platform Management Interface
LED	Light Emitting Diode
MAC	Media Access Controller
MHz	Megahertz
MMC	Module Management Controller
PCIe	Peripheral Component Interconnect Express
PrAMC	Processor AMC
SHLD	Shield
USB	Universal Serial Bus
*u*TCA	Micro Telephony Computing Architecture
XAUI	10 Gigabit Media Independent Interface

Table 1: Acronyms

2 Hardware Overview

2.1 Block Diagram

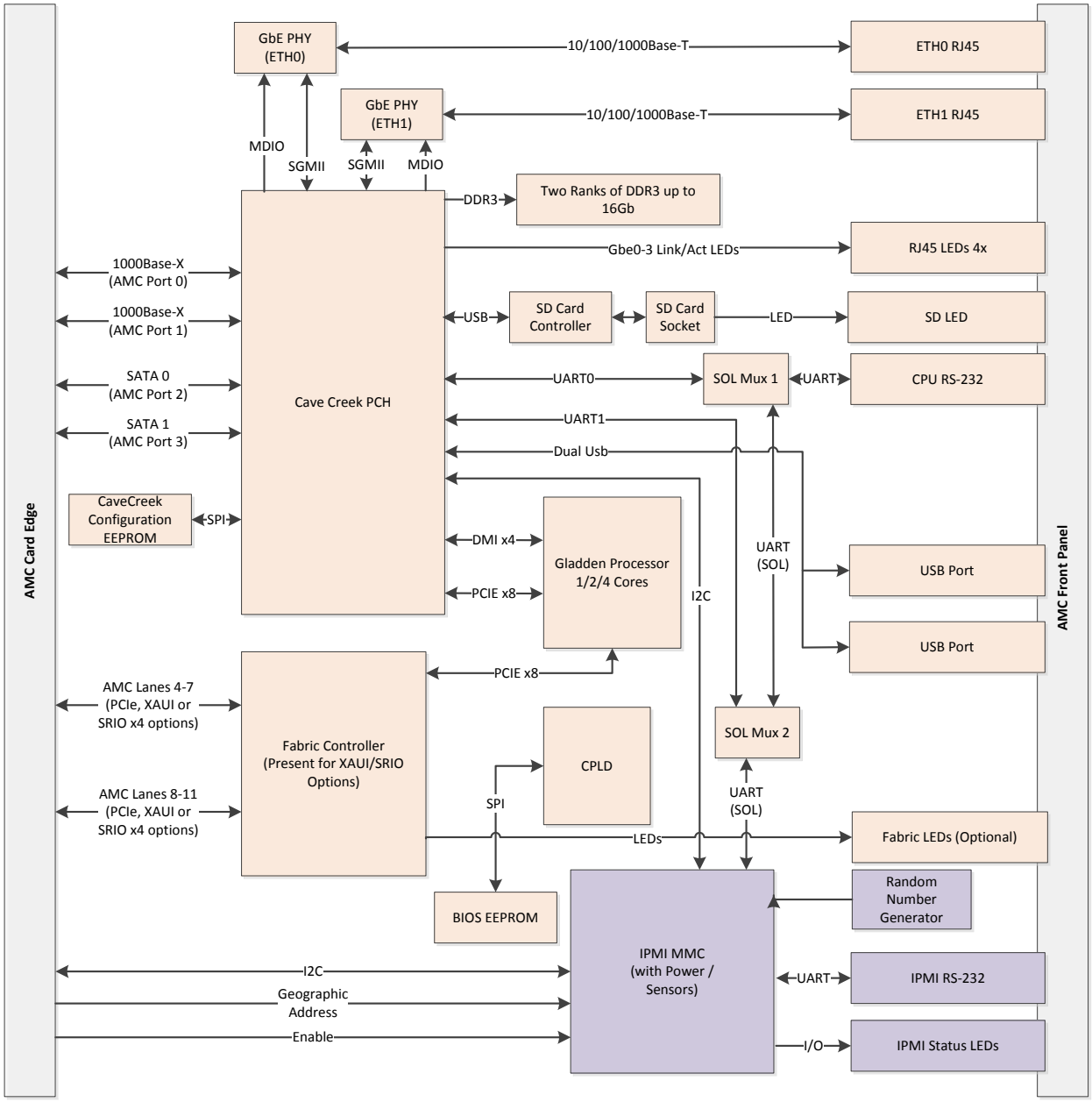

Figure 1: AMC72X (applicable to X=0, 1, 2, and 3) Block Diagram

2.2 Board Layout

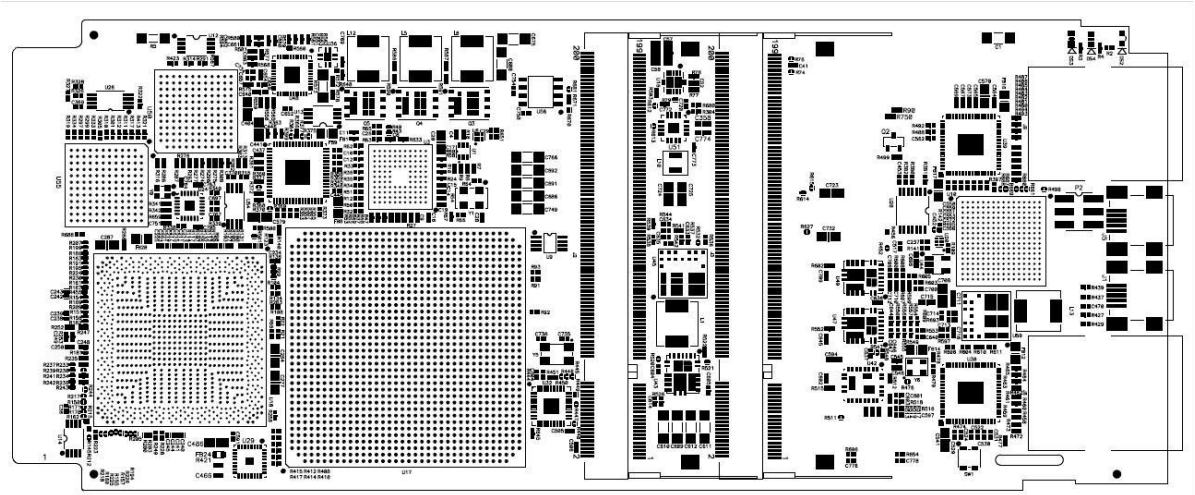

Figure 2: AMC72X Top Layout (front to the left) (X=0, 1, 2, and 3)

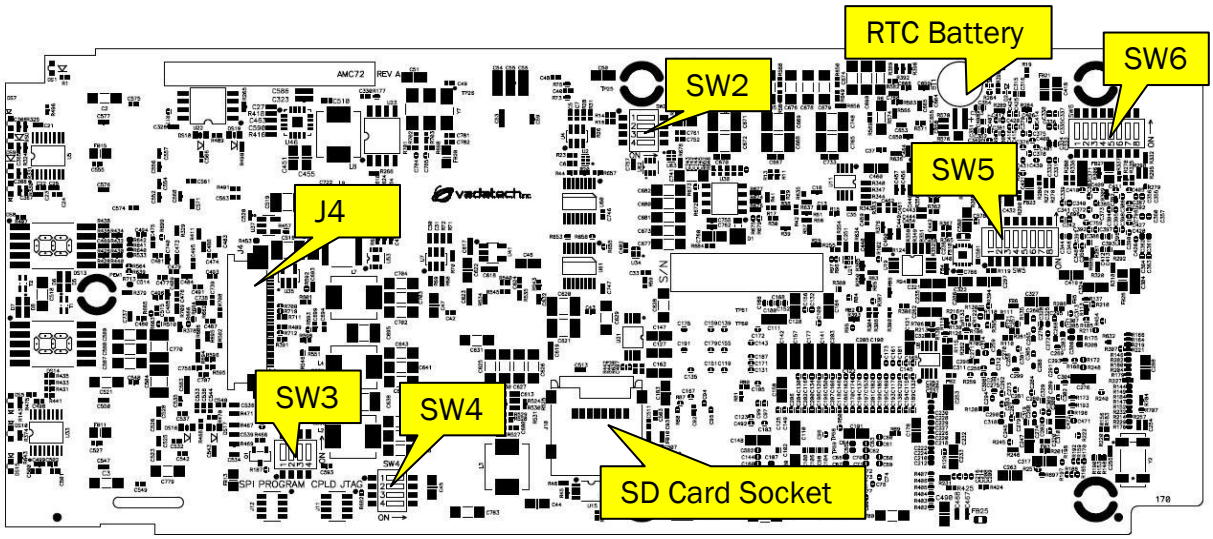

Figure 3: AMC72X Bottom Layout (front to the left) (X=0, 1, 2, and 3)

DIP Switches SW2, SW3, and SW4 are common to all AMC72X boards, switches 5 and 6 are applicable only for AMC722.

SWITCHES	DESCRIPTION
SW2	IPMI Related Functions
SW3	Misc Configuration Switches
SW4	Misc Configuration Switches
SW5	SRIO Ports 4-7 Options
SW6	SRIO Ports 8-11 Options

Table 2: AMC72X Switch configurations

2.3 Front Panel Layouts

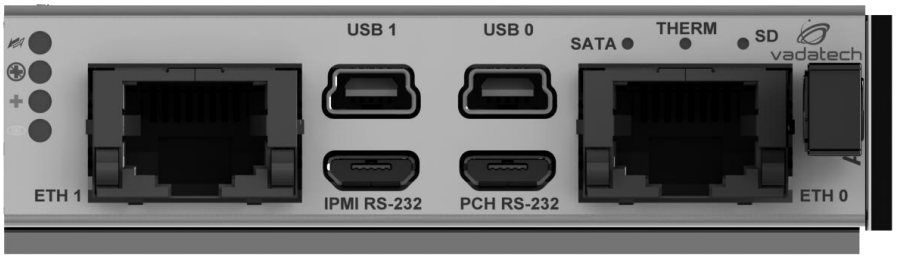

Figure 4: AMC720 Front Panel

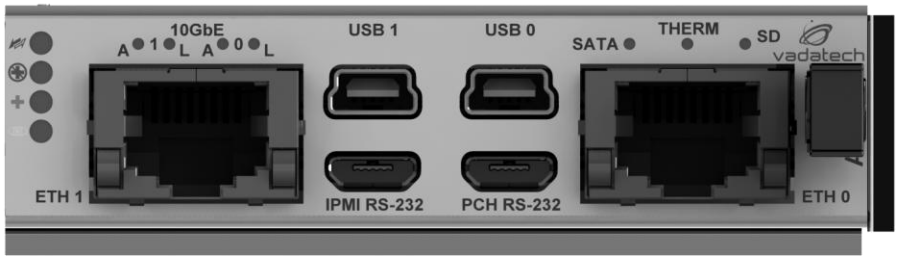

Figure 5: AMC721 Front Panel

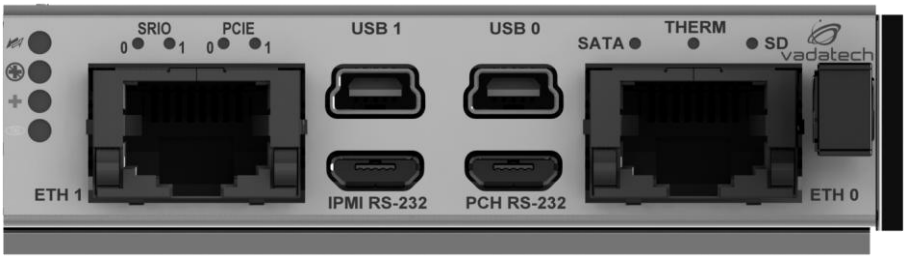

Figure 6: AMC722 Front Panel

Figure 7: AMC723 Front Panel

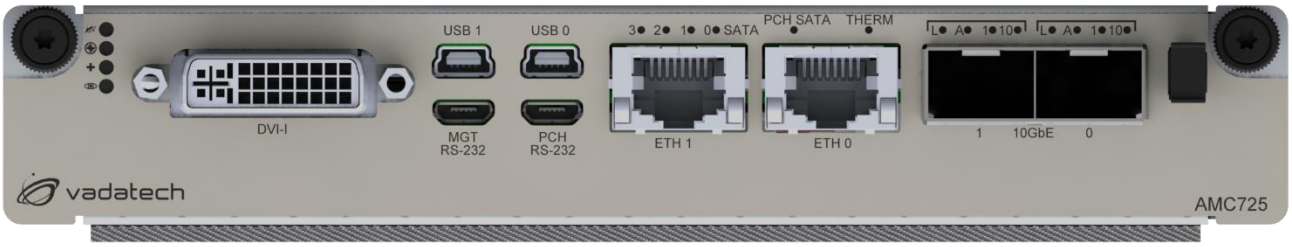

Figure 8: AMC725 Front Panel

2.4 Temperature Sensors

There are four temperature sensors on AMC72X boards. Figure 9 shows the location of temperature sensor on a typical AMC72X board.

Figure 9: Temperature Sensor Location (Bottom Side of AMC72X Board) (X=0, 1, 2, and 3)

3 IPMI Management Interface

The AMC72X has an IPMI Module Management Controller (MMC) which manages the LEDs, module hot-swap handle, e-keying and port status, etc.

The behavior of the IPMI LEDs is as follows:

LED	OFF	ON	BLINK
Blue	Card active	OK to remove	Hot-swap/power transitioning
Red	No Fault	Payload Power Fault	N/A
Green	No management power	Management power OK Payload power OK	Management power OK Payload power not expected
Amber	Normal	Firmware upgrade	N/A

Table 3: AMC LED Behavior

NOTE: The card should only be removed from the chassis when the AMC Blue LED is solid ON.

To insert the card to the chassis, place the card into the carrier's guide rails and push on the front panel firmly until it is fully seated into the connector. If the card does not go fully in, do not force it and instead remove it and check for proper orientation or obstructions. Once fully inserted the Blue LED should go to solid ON while the Green LED should start blinking. Then push in the handle to latch the card into the carrier, the Blue LED should blink for a time and then go solid OFF while the Green LED goes solid ON.

To remove the card, pull out the hot-swap handle until it stops to unlatch the card from the carrier (but do not pull hard enough to remove the card itself yet). The Blue LED should blink for a time and then go solid ON. Once it does, pull the hot-swap handle straight out firmly to remove the card from the carrier.

The AMC72X also has an "IPMI RS-232" connector which enables a serial connection to the IPMI MMC CPU. A VadaTech serial cable assembly is available for connecting to this port which converts the Micro USB form factor into a DB9 connector (VadaTech P/N CBL-DB9MUSB1).

This port operates with 115200-8N1-NOFLOW settings, and the port is pinned out as follows:

Pin	Signal
1	Open
2	Receive
3	Transmit
4	Open
5	Signal GND
SHLD	Chassis GND

Table 4: IPMI RS232 connector pin-out

WARNING: Please take care not to plug USB devices into the "IPMI RS-232" port as there may be a risk of damage. Even though the connector accepts Micro-USB cables, this port is not electrically compatible with USB devices.

3.1 IPMI Internal 10/100 Ethernet

The MMC makes use of CaveCreek PCH Manageability Capability to configure Management Port over one of four 1GbE ports for SOL traffic. This Ethernet port is managed by the MMC and is not accessible to the customer directly. The customer can make use of it indirectly however by using the Serial Over LAN (SOL) functionality of the MMC.

Please refer to the VadaTech MMC and IPMC RMCP and SOL Guide.

4 DIP Switch Settings

The AMC72X products contain numerous DIP switches which will be pre-set by the factory. Some switch settings may need to be changed by the customer in order to match their desired configuration. Factory default settings are marked as blue.

4.1.1 IPMI Related functions

SW2[1:3] control IPMI related functions and are primarily intended for VadaTech use.

Switch	OFF	ON
SW2-1	Factory Default	Reserved
SW2-2	Factory Default	Reserved
SW2-3	Factory Default	Reserved

Table 5: SW2 settings

NOTE: Please do not change the factory default settings unless instructed by VadaTech.

4.1.2 Write Protection Switches

SW2[4] and SW3[1:2] control write protection of various programmable parts available on the board.

Switch	Description	OFF	ON
SW2-4	SD Card Write-Protect	Write-Protected	Writeable
SW3-1	SPI Flash 0 Write-Protect	Writeable	Write-Protected
SW3-2	SPI Flash 1 Write-Protect	Writeable	Write-Protected

Table 6: Write Protection Switch Settings

4.1.3 Board Configuration Switches

SW3[3:4] and SW4 control board relative features which are generic for all AMC72X boards.

Switch	Description	OFF	ON
SW3-3	Don't reboot system on second try.	Reboot After Second Timeout	No Reboot After Second Timeout
SW3-4	PCIe Ref Clock Source	On-Board Clock	Backplane Fabric Clock

SW4-1	RTC Reset	Normal State	Reset Asserted
SW4-2	Secondary RTC Reset	Normal State	Reset Asserted
SW4-3	7-Seg DisplayMode	Bios Post Code	Power State Mode
SW4-4	PCIe Port Bifurcation Strap	x8	Dual x4

Table 7: Board Configuration Switch Settings

Note: SW4-4 is available only on AMC720 since only that board has PCIe on Ports 4-11 and can be configured as dual x4 or single x8 link. Refer to Section IPMI E-Keying Configuration for the steps to configure the module e-keying records for the respective configuration.

4.1.4 SRIO Configuration Switches

SW5 and SW6 are used to configure SRIO on AMC722 ports 4-7 and 8-11.

NOTE: Since both switch SW5 and SW6 settings have exactly the same meaning this section will cover switch configuration only for SW5 keeping in mind that SW6 has the same purpose and applies for second SRIO port.

Switch	Description	OFF	ON
SW5-1	Boot from EEPROM Strap	Disabled	Enabled
SW5-2	Boot from SRIO	After Software sets SRBOOT_CMPL bit	After Fundamental Reset
SW5-3	SRIO Host/Slave Control	SRIO Slave	SRIO Host
SW5-8	Reserved	Factory Default	Reserved

Table 8: SRIO Configuration Switch Settings

SW5[3:4]	Result
ON-ON	BASE_ID = 0xFE LAR_BASE_ID = 0x00FE
ON-OFF	BASE_ID = All Ones LAR_BASE_ID = All Ones

Table 9: SRIO Base Device ID Control Switch Settings

SW5[5:7]	Result
OFF-OFF-OFF	5.0Gbaud
OFF-OFF-ON	2.5Gbaud
OFF-ON-OFF	1.25Gbaud
ON-OFF-ON	3.125Gbaud

Table 10: SRIO Speed Settings

5 Gladden Interface

5.1 Serial Console Port

The AMC72X front panel includes a "CPU RS-232" connector which enables a serial console connection to the CPU using Serial Port 0 exported by CaveCreek PCH. Output redirection to the serial port is configured using BIOS configuration menu. A VadaTech serial cable assembly is available for connecting to this port which converts the Micro USB form factor into a DB9 connector (VadaTech P/N CBL-DB9MUSB1).

This port operates with 9600-8N1-NOFLOW settings; the port is pinned as follows:

Pin	Signal
1	Open
2	Receive
3	Transmit
4	Open
5	Signal GND
SHLD	Chassis GND

Table 11: CPU RS232 connector pin-out

WARNING: Please take care not to plug USB devices into the "CPU RS-232" port as there may be a risk of damage. Even though the connector accepts Micro-USB cables, this port is not electrically compatible with USB devices.

NOTE: This RS-232 port is not available during the time that a Serial Over LAN (SOL) session is active to the board using Serial Port 0 since during that time the Serial Port 0 is automatically switched away from the front panel and is connected to the MMC so that it can convey the serial traffic via Ethernet.

5.2 USB Ports

The AMC72X front panel includes two USB ports. USB Ports are connected to the CaveCreek USB Ports 0 and 1. A USB device may be attached to this port for expansion.

Pin	Signal
1	+5V
2	D-
3	D+
4	Open
5	Signal GND
SHLD	Chassis GND

Table 12: USB port pin-out

5.3 1GbE Ports

There are two 10/100/1000Base-T (copper) Ethernet ports available on the front panel. ETH0 and ETH1 are attached to the CaveCreek 1GbE ports 2 and 3 via two 88E1114 PHYs.

Dedicated 1000Base-X Ports are connected to CaveCreek 1GbE Ports 0 and 1 and then to AMC Ports 0 and 1.

The LEDs on the RJ45 ports on the front panel replicate the state of four 1Gbe ports exported by CaveCreek. The LEDs for those ports are defined as follows:

LED	ON	OFF	BLINK
Green	GbE2 Linked	GbE2 not linked	GbE2 Activity
Orange	GbE0 linked	GbE0 not linked	GbE0 Activity

Table 13: ETH0 LEDs

LED	ON	OFF	BLINK
Green	GbE3 Linked	GbE3 not linked	GbE3 Activity
Orange	GbE1 linked	GbE1 not linked	GbE1 Activity

Table 14: ETH1 LEDs

5.4 XAUI Ports (only applicable to AMC721 and AMC723)

Depending on the board model, there are up to two available XAUI ports on the backplane. AMC721 provides XAUI ports on AMC 4-7 and AMC 8-11, while AMC723 only provides a single XAUI port on AMC 8-11.

The LEDs on the front panel on both of these AMC modules provide indication of Link and Activity for the available ports per the following table:

LED	ON	OFF	BLINK
A	n/a	No activity	Activity
L	Corresponding port linked	Corresponding port not linked	n/a

Table 15: 10GbE LEDs

5.5 SRIO Ports (only applicable to AMC722)

AMC722 provides dual SRIO x4 interface on backplane lanes 4-7 and 8-11. Since the SRIO interface is available via a PCIe-to-SRIO Bridge, front panel LEDs reflect the current state of both sides of the bridge, hence the SRIO and PCIE LEDs above ETH 1 connector.

Such LEDs are defined as follows:

LED	ON	OFF	BLINK
SRIO 0/1	Corresponding SRIO port detected reset	Normal Function	n/a
PCIE 0/1	Corresponding PCIe port detected Hot Reset	Normal Function	n/a

Table 16: SRIO Bridge LEDs

5.6 SD Card Socket

The AMC72X board includes a Micro SD card socket. This socket connects to the Gladden by way of a USB2244 USB SD media controller chip. This SD card is typically used to hold the kernel and root file-system. This socket has a front panel LED associated with it as follows:

LED	Color	ON	OFF	BLINK
SD	Green	n/a	No activity	Activity

Table 17: SD Card LED

5.7 CaveCreek EEPROM

An AT25128B EEPROM is provided on the CaveCreek EEPROM port. This EEPROM is delivered with factory programmed image which contains default PCIe configuration space and CaveCreek GbE register settings. This EEPROM can be customized using Intel EEPROM Image Creation Tool (EICT). To flash the EEPROM image use Intel eepdate tool.

5.8 DDR3 SO-DIMMs

The board comes pre-loaded with either 4GB, 8GB, or 16GB of DDR3 memory with ECC depending on ordering option "B". The memory is carried on VadaTech proprietary SO-DIMMs and inserted in slots J2 and J3 on the board. The software uses the SO-DIMM's SPD EEPROMs to determine the size and type of memory.

Slot	Chip Select	Data Width	TWSI0 SPD EEPROM
J2	*DDR_DIMM0_CS0	64-bit + 8-bit ECC	"1010010"
	*DDR_DIMM0_CS1		
J3	*DDR_DIMM1_CS0		"1010001"
	*DDR_DIMM1_CS1		

Table 18: DDR3 SO-DIMM mapping

5.9 Ethernet PHY Addressing

The AMC72X board includes two 1GbE PHYs.

PHY Address	Type	Port
0x01	88E1114	1GbE ETH0
0x02	88E1114	1GbE ETH1

Table 19: Gladden Ethernet PHY Addressing

NOTE: The backplane 1GbE ports and XAUI ports (if applicable) do not have a PHY; 1GbE ports are connected from CaveCreek PCH chip to the backplane without going through a PHY.

6 Software

The AMC72x comes pre-configured with AMI Aptio BIOS installed in the SPI flash devices, and Fedora installed in the on-board micro SD card.

6.1 BIOS

The BIOS is AMI Aptio version 4.6.5.4; it is based on the Intel Stargo Customer Reference Board with modifications to support the AMC72x hardware.

Setup Menu

After a power cycle or reset, the BIOS will present a welcome screen via the PCH serial port. Pressing the Del key causes the Setup Menu to be displayed. From Setup the customer may modify the BIOS settings as needed; for example the Boot menu is used to modify the boot device order.

Updating the BIOS

The Intel Flash Programming Tool, FPT is used to re-flash the BIOS firmware. Another option is to use the AMI AFU utility to re-flash the BIOS with a new image. Versions for DOS, Windows, and EFI are available to download from AMI.

Here are the steps on how to re-flash BIOS using AMI AFU tool:

1. Download AMI AFU utility from the link above and extract on host PC
2. Go to `amflash/Aptio/AFUEFI`
3. Go to `32` or `64` depending on CPU
4. Open the archive file and copy .efi file to USB Flash Disk
5. Download upgrade image from Vadatech on following link
   `username: customer`
   `password: amc72xvt@72`

6. Disconnect USB Flash from host PC and connect to AMC72X
7. Select EFI shell from BIOS boot menu and boot to EFI
8. USB Flash should show up as `fs0`
9. Enter `fs0:` command to open USB Flash
10. Use following command to upgrade bios:
    `<efi_file_name.efi> <bios_file_name> /P`
11. After upgrade is done, power cycle the board

Network Boot (PXE)

To enable booting via the network (PXE boot) following steps should be performed:

1. Enter BIOS
2. Go to Advanced/Network Stack
3. Enable Network stack and make sure that Ipv4 PXE Support and Ipv6 PXE Support are enabled
4. Save changes and exit
5. Power cycle the board and enter BIOS
6. Go to Boot menu
7. Enter CSM Parameters submenu
8. Set Launch PXE OpROM poli to [Legacy first]
9. Save changes and exit
10. Power cycle the board and enter BIOS
11. Go to Boot menu
12. If your NBP (Network Bootstrap Program) does not support UEFI and Legacy mode is preferred then perform following steps

    a) Go to Network Device BBS Priorities
    b) You should see following devices
    IBA GE Slot 0101 v1350 (AMC port 0)
    IBA GE Slot 0102 v1350 (AMC port 1)
    IBA GE Slot 0103 v1350 (Front port 0)
    IBA GE Slot 0104 v1350 (Front port 1)

    c) Set Boot Option #1 the device which is connected to the network which has PXE server
    d) Exit submenu

13. Under Boot Option Priorities choose IBA GE Slot 010X v1350 if preferred to use legacy mode, or one of UEFI devices below, depending on which port is connected to the network with PXE server

    UEFI: IP4 Intel(R) DH8900CC Series Gigabit Backplane Network Connection (AMC port 0)
    UEFI: IP6 Intel(R) DH8900CC Series Gigabit Backplane Network Connection (AMC port 0)
    UEFI: IP4 Intel(R) DH8900CC Series Gigabit Backplane Network Connection (AMC port 1)
    UEFI: IP6 Intel(R) DH8900CC Series Gigabit Backplane Network Connection (AMC port 1)
    UEFI: IP4 Intel(R) DH8900CC Series Gigabit Network Connection (Front port 0)
    UEFI: IP6 Intel(R) DH8900CC Series Gigabit Network Connection (Front port 0)
    UEFI: IP4 Intel(R) DH8900CC Series Gigabit Network Connection (Front port 1)
    UEFI: IP6 Intel(R) DH8900CC Series Gigabit Network Connection (Front port 1)

14. Save changes and exit

After reboot AMC72X will try to locate PXE server and try to boot from it if present.

Boot Devices

To modify the boot device order, select the Boot tab and scroll down to Boot Option Priorities. Select the Boot Option number and change it by selecting from the list in the dialog box.

6.2 Linux

The AMC72x comes pre-programmed with Fedora installed in the on-board SD card. Linux includes many different commands and features, which cannot all be described here. Additional documentation resources can be found on-line at fedoraproject.org and on other Linux resource site.

Logging In

The PCH serial port is used to log-in to Linux using the 9600 8N1 settings. At the log-in prompt you should see the following:

```
Fedora release 18 (Spherical Cow)
Kernel 3.9.4-200.fc18.x86_64-vt on an x86_64 (/dev/ttyS0)

localhost login: root
Password: rootroot
```

Log-in as root using the password as shown above. You may change the root password after logging-in.

Network Device Mapping

The AMC72x family devices have four 4 GbE interfaces 2 of them routed to front Ethernet ports, two of them routed to AMC Ports 0 and 1. XAUI ports are present on AMC Ports 4-7 and 8-11 depending on particular product. For more information refer to tables below.

Interface	Default IP Address	Type	Port
eth0	192.168.40.212	GbE	AMC Port 0
eth1	192.168.41.212	GbE	AMC Port 1
eth2	192.168.1.199	GbE	Front Port 0
eth3	192.168.2.199	GbE	Front Port 1

Table 20: AMC720 and AMC722 Network Device Mapping

Interface	Default IP Address	Type	Port
eth0	192.168.42.212	XAUI	AMC Ports 4-7
eth1	192.168.43.212	XAUI	AMC Ports 8-11
eth2	192.168.40.212	GbE	AMC Port 0
eth3	192.168.41.212	GbE	AMC Port 1
eth4	192.168.1.199	GbE	Front Port 0
eth5	192.168.2.199	GbE	Front Port 1

Table 21: AMC721 Network Device Mapping

Interface	Default IP Address	Type	Port
eth0	192.168.42.212	XAUI	AMC Ports 8-11
eth1	N/A	N/A	Not Connected
eth2	192.168.40.212	GbE	AMC Port 0
eth3	192.168.41.212	GbE	AMC Port 1
eth4	192.168.1.199	GbE	Front Port 0
eth5	192.168.2.199	GbE	Front Port 1

Table 22: AMC723 Network Device Mapping

NOTE: Only first 10GbE port is connected to AMC Ports. Second port is unconnected and shows up as a dummy port in Linux. It cannot be used.

VNC Server

The Linux GUI can be accessed remotely over the network since there is a VNC server installed in the Linux. The server is preconfigured and ready to use, but it is off by default. Use the command bellow to start VNC server:

```
# vncserver :1 -geometry 800x600 -depth 24
```

The following command stops VNC server:

```
# vncserver -kill :1
```

The password for VNC server is same as password for root user.

6.3 Graceful Shutdown Support

Graceful shutdown provides a way of gracefully shutting down the OS running on the board once payload deactivation request from uTCA Carrier is received due to explicit deactivation command or AMC handle opened.

Graceful shutdown a result of cooperation of different components of AMC design which are described below:

1. IPMI Controller supports
    a. OEM IPMI commands which allow the user to enable/disable graceful shutdown support
    b. Read the Quiesced state of the AMC to determine whether AMC deactivation has been requested by uTCA Carrier Manager
    c. Monitor of CPU power state to detect system shutdown completion
2. Hardware support
    a. I2C path to payload CPU which enables OS communication to IPMI Controller
3. Application running on OS side
    a. Performs AMC Quiesced state monitoring through i2c using OEM IPMI commands and gracefully shuts down the OS once deactivation is requested by uTCA Carrier Manager.

NOTE: OS side Graceful shutdown support is OS specific and the user should implement its own way of shutting down the board using provided interface and OEM IPMI commands. Vadatech has the Graceful shutdown support in place for Fedora Linux available on SD Card shipped with the board.

6.3.1 Implementing Graceful Shutdown

In order to implement graceful shutdown support in the OS following stuff is required:

1. Driver to be able to communicate on payload i2c bus
2. Interface for sending IPMI packets over i2c bus

By default IPMI controller is initialized with graceful shutdown support disabled allowing proper operation of operating systems which do not implement graceful shutdown.

After OS starts graceful shutdown support should be enabled by the software using IPMI "Set Graceful Shutdown" OEM command.

After enabling graceful shutdown the software should continuously monitor Quiesced state of the AMC by issuing IPMI "Get Quiesced State" OEM command.

Once AMC goes to "Quiesce In Progress" state the software should start OS shutdown. IPMI controller will monitor CPU power state and will report that payload has been turned off to uTCA carrier once CPU goes to power down state.

Name	NetFn	Cmd	Input Data	Output Data
Set Graceful Shutdown	0x2e	0x37	byte[0] = 0x32 byte[1] = 0x5d byte[2] = 0x00 byte[3] = *value* *value*: 0 - Disable 1 - Enable	byte[0] = IPMI CompCode byte[1] = 0x32 byte[2] = 0x5d byte[3] = 0x00
Get Quiesced State	0x2e	0x38	byte[0] = 0x32 byte[1] = 0x5d byte[2] = 0x00	byte[0] = IPMI CompCode byte[1] = 0x32 byte[2] = 0x5d byte[3] = 0x00 byte[4] = *value* *value*: 0 - Not Quiesced 1 - Quiesce in Progress 2 - Quiesced

Table 23: Graceful Shutdown IPMI OEM Commands

7 IPMI E-Keying Configuration

An AMC E-Keying menu is available via the IPMI RS-232 port for AMC720 and AMC722. This e-keying configuration is already performed at the factory to match the ordering options of the board. However, this menu can be accessed if desired to turn on/off sets of backplane e-keying records for the GbE, PCIe, SRIO and SATA ports.

To use the menu system simply follow the on-screen directions to enable/disable the various sets of e-keying records. When a set of records is enabled it will have an asterisk next to it and when it is disabled it will not have the asterisk.

After configuring e-keying please remove and reinsert the card to ensure that the carrier manager correctly re-reads the contents of the e-keying records.

Following tables map switch settings to suggested e-keying configuration.

SW4-4	Active E-Keying options	Result
OFF	1, 2, 3, 5, 6, 7	PCIe x8
ON	1, 2, 3, 4, 6, 7	PCIe Dual x4

Table 24: AMC720 E-Keying Configuration

SW5[5:7]	Active E-Keying options	Result
OFF-OFF-OFF	1, 2, 3, 7, 11, 12	5.0Gbaud
OFF-OFF-ON	1, 2, 5, 9, 11, 12	2.5Gbaud
OFF-ON-OFF	1, 2, 6, 10, 11, 12	1.25Gbaud
ON-OFF-ON	1, 2, 4, 8, 11, 12	3.125Gbaud

Table 25: AMC722 E-Keying Configuration

8 Serial Over Lan (SOL)

The Serial Over Lan function can redirect the CPU RS-232 serial ports into an SOL network session. When using `serial0` as SOL serial port software will redirect the port from front panel to SOL session. This allows for straightforward remote access to the CPU console serial port without the need for having an RS-232 cable connected to the serial port.

CaveCreek exports two serial ports (`serial0` and `serial1`). Configuration command is available on IPMI RS-232 port to select serial port for SOL using `plser` command.
One of four 1GbE ports can be configured as a management port to direct SOL traffic. This option is software configurable and can be modified using `mgtport` command to select one of two backplane ports (`back0` and `back1`) or one of two front panel ports (`front0` and `front1`) as management port.

A separate manual is available describing additional functionality. Please refer to the VadaTech MMC and IPMC RMCP and SOL Guide.

9 Factory Setup

9.1 Initial Factory Setup

The MAC addresses for the board should already be configured by VadaTech during manufacturing. Take care not to erase CaveCreek EEPROM so as not to lose the globally unique MAC addresses that have been assigned.

In the factory these MAC addresses are assigned as follows:

1) TARGET: Boot DOS using bootable USB Flash Stick
2) PC: Reserve 5 MAC addresses from the VadaTech MAC pool for each 1Gbe ports plus 1 port for IPMI/SOL Management traffic
3) TARGET: Use **`eeupdate`** tool to set MAC addresses.

NOTE: Management port will automatically assign itself 5th reserved MAC address.

NOTE: The board must be power-cycled or reset after setting the MAC address before it will take effect.

For AMC721 and AMC723 same steps should be performed to update MAC addresses on XAUI ports.

9.2 Writing the Factory Default SD Card Contents

An image is provided in the BSP release package to restore the default SD Card contents. Writing this image to an SD Card will entirely wipe out the contents of the SD Card.

WARNING: ***Use care to specify the correct /dev/sd device under Linux as using the wrong device could result in wiping out the contents of your PC's hard drive! USE EXTREME CAUTION WHEN PERFORMING THESE STEPS AND ENSURE THAT YOU UNDERSTAND WHAT IS ABOUT TO HAPPEN BEFORE MOVING ON…***

1) Linux PC: Insert the SD Card from the AMC72X into an SD Card reader on your Linux PC.
2) Linux PC: Determine which device Linux has assigned to the SD Card. Your hard drive is probably /dev/sda so **DON'T** use that one or your will wipe out your hard drive. The SD Card will usually be /dev/sdb or /dev/sdc, etc depending on how many hard drives are already in your system. Note that this assignment may change over time as you add/remove hard drives or memory cards from your system so it is important to check each time.
3) Linux PC: **`dd if=amc72`*`X`*`_sd_card_`*`Y`*`gb.img of=/dev/sd`*`Z`*

NOTE: *X* specifies the exact product form AMC72X family. Specify *Y* as the density of the SD card. Specify *Z* as the identifier of the SD Card as assigned by Linux. Do not specify any numeric suffix as the image is a full disk image and includes multiple partitions. It should be written to the raw drive device not a partition device.

Expect the copying process to take around a half an hour.

10 AMC725 Specific Changes

The AMC725 is the latest in AMC72x series of Processor AMCs. This section describes the key differences between the AMC725 from AMC720, 1, 2, and 3.

10.1 Block Diagram

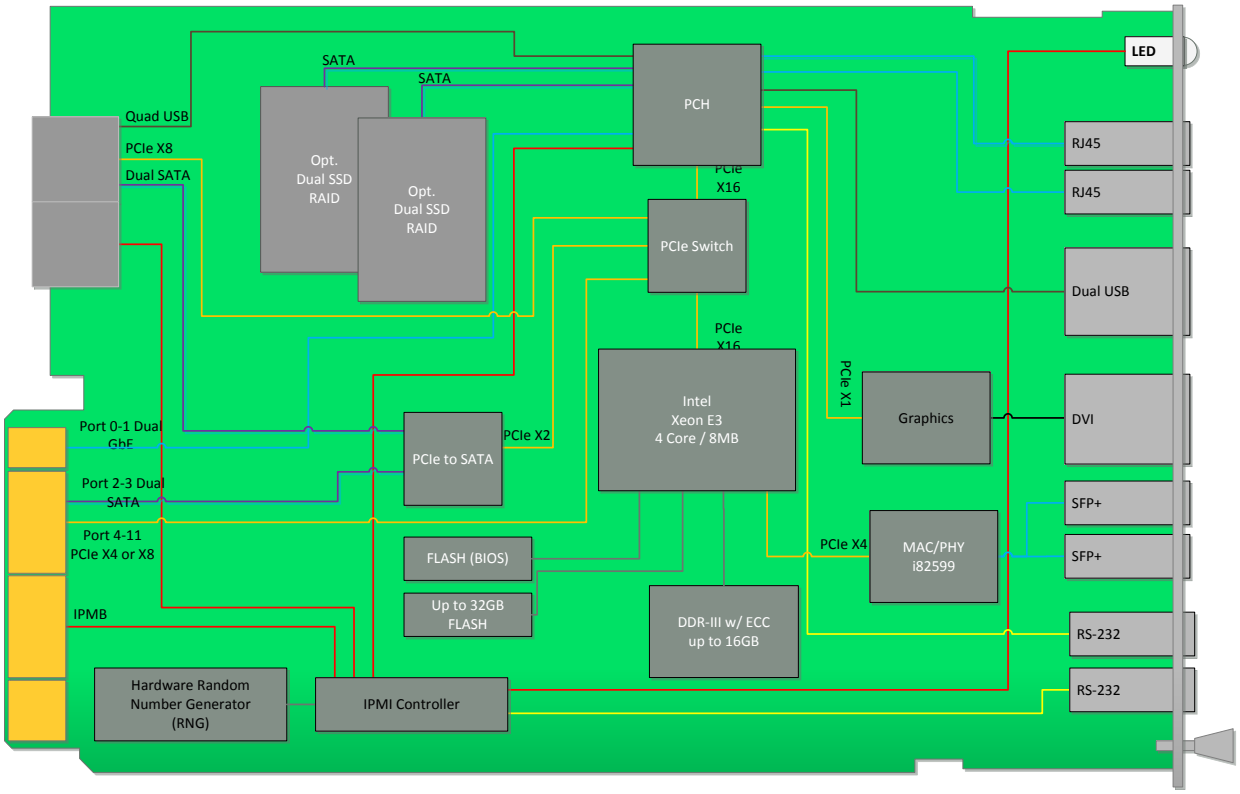

Figure 10: AMC725 Block Diagram

10.2 Summary

The summary of key differences in AMC725 compared to the other AMC72x devices are:

- AMC725 is a double-width, mid-height Advanced Mezzanine Card, with options for full-height.
- AMC725 has a built-in graphics controller, routed to the front panel through the DVI-I connector
- Support for two SATA disk drives (one on the baseboard and other on an optional daughter board)

- AMC725 supports additional peripherals and interfaces compared to other AMC72x device and to support these additional features a PCIe Gen 3 switch is used
- Ports 4 to 11 on AMC725 are routed from the PCIe Gen 3 switch to the backplane connectors
- From the PCIe Gen3 Switch:
  - PCIe x16 to PCH
  - PCIe x16 to CPU
  - PCIe x8 to RTM connector
  - PCIe x1 to Graphics controller
  - PCIe x2 to SATA controller, which controls the Ports 2 and 3
- The 10GbE NIC on AMC725 is routed to the front panel through dual SFP+ connectors
- µRTM Connector provides the following interfaces:
  - 4x USB from PCH
  - PCIe x8 from PCIe Gen3 Switch
  - 2x SATA ports
  - 2x PCIe reference clocks

10.3 Switches and Sensors

The location on switches and temperature sensors on AMC725 are shown below.

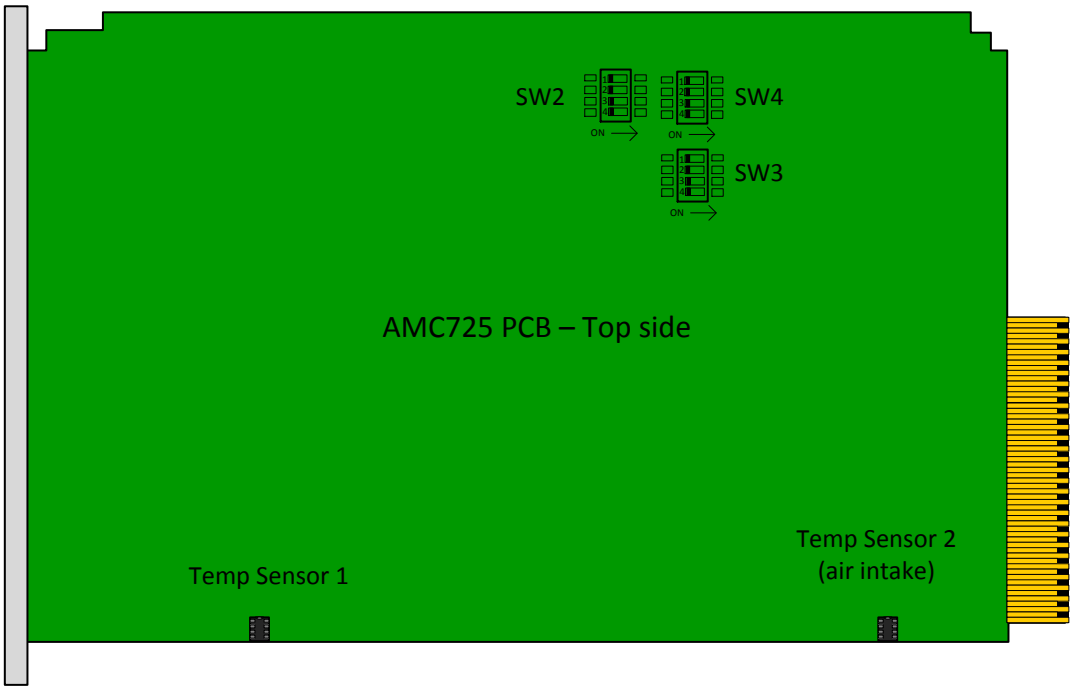

Figure 11: AMC725 PCB Top Side

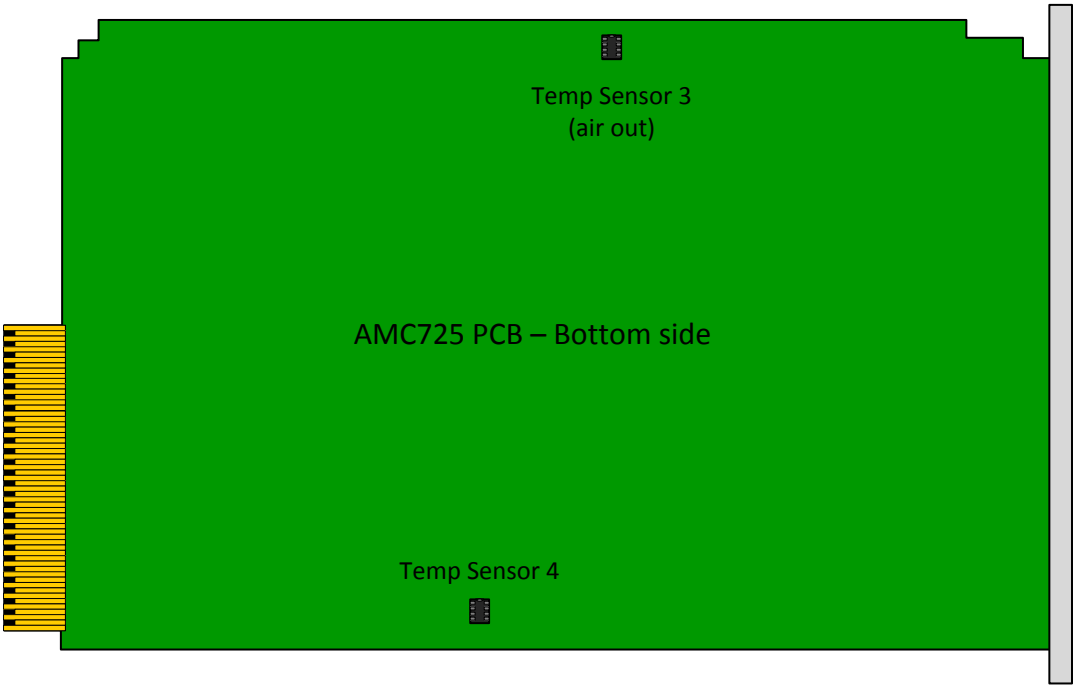

Figure 12: AMC725 PCB Bottom Side